Date Mailed: August 10, 2004

Sheet 1 of 1

FORM 1449* INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION (Use several sheets if necessary)	Docket Number: 50019.273US01/P05808	Application Number: 10/808,635
	Applicant: Siew Siong Teo	
	Filing Date: March 24, 2004	Group Art Unit: ~~2830~~ 2816

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TLE	6,075,354	6/13/00	Smith et al.	323	313	
TLE	US 6,183,131 B1	2/6/01	Holloway et al.	374	172	
TLE	US 6,232,828 B1	~~5/15/01~~ 5/15/01	Smith et al.	327	539	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TLE		Randall L. Geiger et al., "VLSI Design Techniques for Analog and Digital Circuits," 1990 ~~(2 pages)~~ (p 369)
TLE		Phillip E. Allen et al., "CMOS Analog Circuit Design," 1987 ~~(3 pages)~~ (pp 591 and 595)

EXAMINER /Terry Englund/	DATE CONSIDERED 09/06/2006

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form for next communication to the Applicant.